

Agilent E9521A **ARM7/9/11 ETM** Decoder

Design Guide



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In This Guide...

This *Design Guide* provides information to assist you in designing a board which will be compatible with the Agilent E9521A ARM7/9/11 ETM Decoder. It tells you what signals are required by the decoder, and suggests how to route these signals to a header.

For information on using the decoder, see the online help which is installed with the decoder.

Product Overview

The ARM7/9/11 ETM Decoder, used with an Agilent Technologies logic analyzer, allows you to view instructions and messages that are executing in your target system.

The decoder can decode 8-, 16-, and 32-bit wide data. It disassembles ARM and Thumb instructions, but not Jazel instructions.



Target System Requirements

The decoder has been designed to work with target systems meeting the following requirements:

Supported processor

- ARM7 processor with ETM v1.1 v1.2
- ARM9 processor with ETM v1.0 v1.3
- ARM11 processor with ETM v3.1

Object files

• You must have access to the object files for the code which is executing on your target system.

Supported compilers

• ARM RealView Developer's Suite 2.1, or a compiler which generates object files with an equivalent ELF object file format.

Headers

• You must provide MICTOR headers, as described in this guide, to connect the logic analyzer probes to the signals on your target system.

Equipment Required

Logic analysis system

You need an Agilent 16900-series or 1680/90-series logic analyzer.

Logic analyzer cards

The logic analyzer card(s) you use must support the speed of the bus you are probing.

The logic analyzer card(s) must provide enough channels to probe the headers on your target system.

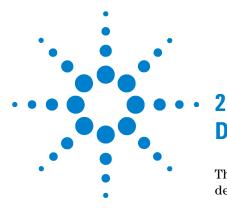
Probing scheme	Number of channels			
ETM-8 or ETM-16, 1 MICTOR connector	32			
ETM-32, 2 MICTOR connectors	48			

 Table 1
 Logic analyzer channels required

Probes

You need an appropriate number of logic analyzer probes ("adapter cables") to connect the logic analyzer cables to the headers on your target system. The probe must match the type of connector you have placed on your board. Agilent recommends a MICTOR connector and an Agilent E5346A or E5380A probe.

1 Introduction



Designing Your Board

This chapter describes the factors you need to consider when designing and preparing your target system for logic analysis.

Overview of the Connectors

You must provide one or two AMP MICTOR 38 connectors with the signal mappings shown in the following sections. Use connector J1 if you have 8 bits or 16 bits of TRACEDATA. Use connectors J1 and J2 if you have 32 bits of TRACEDATA.

You may also need to provide a 2x10 berg connector for JTAG-only signals. See "Sharing the Connector Between Multiple Tools" on page 20 for more information on this connector.



Designing the Headers

AMP MICTOR 38 connectors

The signal-to-connector mappings shown in this chapter assume you are using AMP MICTOR 38 connectors.

Each MICTOR 38 connector carries 32 signals plus two clocks (CLK1 for two logic analyzer pods). Probes (part number E5346A, sometimes called "high-density termination cables") are required to connect the logic analyzer cables to the MICTOR connector. These probes contain the required termination. One probe is required for every two logic analyzer pods.

To increase the structural support for the probes, you should use support shrouds on each connector.

For more information, including mechanical dimensions, see the *Agilent Technologies E5346A 38-Pin Probe and E5351A 38-Pin Adapter Cable Installation Note*, available from www.agilent.com.

Design Considerations

The connector must be close enough to the signal source so that the stub length created is less than $^{1}\!/_{5}$ the t_{r} (bus risetime). For PC board material, (er = 4.9) and Z_{o} in the range of 50 - 80 Ω , use a propagation delay of 160 ps/inch of stub.

Each probed signal line must be able to supply a minimum of 600 mV to the probe tip and handle a minimum of 90 k Ω shunted by 10 pF. The maximum input voltage to the logic analyzer is $\pm 40V$ peak

Connectors for ARM11

J1: ARM11 ETM Signals for Agilent Logic Analysis and ARM RealView Trace

J1 is designed to be used either with an Agilent logic analyzer *or* with ARM's RealView Trace. When J1 is used with the logic analyzer, the JTAG (run control) signals (shaded in blue) must be routed to a separate JTAG-only connector (page 20) so they are accessible to a JTAG controller such as ARM RealView ICE.

The signals shaded in blue are used by RealView Trace, but are not used by the logic analyzer.

Analyzer Pod	ETM Signal		r pin # view)		TM Signal	Analyzer Pod
5V		-	2			
•••	NC	1	_		NC	
5V	NC	3	4		NC	12C
CLK even	GND	5	6		TRACECLK	CLK odd
D15 even	DBGRQ	7	8	MRI	DY or DBGACK	D15 odd
D14 even	nSRST	9	10		EXTTRIG	D14 odd
D13 even	TDO	11	12		VTRef	D13 odd
D12 even	RTCLK	13	14		Vsupply	D12 odd
D11 even	ТСК	15	16	TF	RACEDATA 7	D11 odd
D10 even	TMS	17	18	TF	RACEDATA 6	D10 odd
D9 even	TDI	19	20	TF	RACEDATA 5	D9 odd
D8 even	nTRST	21	22	TF	RACEDATA 4	D8 odd
D7 even	TRACEDATA 15	23	24	TF	RACEDATA 3	D7 odd
D6 even	TRACEDATA 14	25	26	TF	RACEDATA 2	D6 odd
D5 even	TRACEDATA 13	27	28	TF	RACEDATA 1	D5 odd
D4 even	TRACEDATA 12	29	30	GND	or EXTOUT1	D4 odd
D3 even	TRACEDATA 11	31	32	GND	or EXTOUT0	D3 odd
D2 even	TRACEDATA 10	33	34		VDD	D2 odd
D1 even	TRACEDATA 9	35	36		TRACECTL	D1 odd
D0 even	TRACEDATA 8	37	38	TF	RACEDATA 0	D0 odd

J2: ARM11 upper ETM signals for logic analysis

This header is required only if the ETM core is set up to collect 32 bits of TRACEDATA.

5V NC 1 2 NC 12C 5V NC 3 4 NC 12C CLK even NC 5 6 NC CLK odd D15 even NC 7 8 TRACEDATA 31 D15 odd D14 even NC 9 10 TRACEDATA 30 D14 odd D13 even NC 11 12 TRACEDATA 29 D13 odd D12 even NC 13 14 TRACEDATA 28 D12 odd D11 even NC 15 16 TRACEDATA 28 D12 odd D10 even NC 17 18 TRACEDATA 26 D10 odd D9 even NC 21 22 TRACEDATA 25 D9 odd D8 even NC 23 24 TRACEDATA 23 D7 odd D6 even NC 25 26 TRACEDATA 21 D6 odd D5 even NC 27 28 TRACEDATA 20 D4 odd D3 even <th>Analyzer Pod</th> <th>ETM Signal</th> <th></th> <th>r pin # view)</th> <th>ETM Signal</th> <th>Analyzer Pod</th>	Analyzer Pod	ETM Signal		r pin # view)	ETM Signal	Analyzer Pod
CLK evenNC56NCCLK oddD15 evenNC78TRACEDATA 31D15 oddD14 evenNC910TRACEDATA 30D14 oddD13 evenNC1112TRACEDATA 29D13 oddD12 evenNC1314TRACEDATA 28D12 oddD11 evenNC1516TRACEDATA 27D11 oddD10 evenNC1718TRACEDATA 26D10 oddD9 evenNC1920TRACEDATA 25D9 oddD8 evenNC2324TRACEDATA 23D7 oddD6 evenNC2728TRACEDATA 21D5 oddD5 evenNC2728TRACEDATA 20D4 oddD3 evenNC3132TRACEDATA 19D3 oddD2 evenNC3334TRACEDATA 17D1 odd	5V	NC	1	2	NC	12C
D15 evenNC78TRACEDATA 31D15 oddD14 evenNC910TRACEDATA 30D14 oddD13 evenNC1112TRACEDATA 29D13 oddD12 evenNC1314TRACEDATA 28D12 oddD11 evenNC1516TRACEDATA 27D11 oddD10 evenNC1718TRACEDATA 26D10 oddD9 evenNC1920TRACEDATA 25D9 oddD8 evenNC2122TRACEDATA 23D7 oddD6 evenNC2324TRACEDATA 22D6 oddD5 evenNC2728TRACEDATA 21D5 oddD4 evenNC2930TRACEDATA 20D4 oddD3 evenNC3132TRACEDATA 19D3 oddD2 evenNC3334TRACEDATA 17D1 odd	5V	NC	3	4	NC	12C
D14 even NC 9 10 TRACEDATA 30 D14 odd D13 even NC 11 12 TRACEDATA 29 D13 odd D12 even NC 13 14 TRACEDATA 29 D13 odd D11 even NC 13 14 TRACEDATA 28 D12 odd D10 even NC 15 16 TRACEDATA 26 D11 odd D10 even NC 17 18 TRACEDATA 26 D10 odd D9 even NC 19 20 TRACEDATA 25 D9 odd D8 even NC 21 22 TRACEDATA 24 D8 odd D7 even NC 23 24 TRACEDATA 23 D7 odd D6 even NC 25 26 TRACEDATA 21 D5 odd D4 even NC 29 30 TRACEDATA 20 D4 odd D3 even NC 31 32 TRACEDATA 19 D3 odd D2 even NC 33 34 TRACEDATA 17 D	CLK even	NC	5	6	NC	CLK odd
D13 even NC 11 12 TRACEDATA 29 D13 odd D12 even NC 13 14 TRACEDATA 28 D12 odd D11 even NC 15 16 TRACEDATA 27 D11 odd D10 even NC 17 18 TRACEDATA 26 D10 odd D9 even NC 19 20 TRACEDATA 25 D9 odd D8 even NC 23 24 TRACEDATA 23 D7 odd D6 even NC 25 26 TRACEDATA 22 D6 odd D5 even NC 29 30 TRACEDATA 21 D5 odd D4 even NC 29 30 TRACEDATA 20 D4 odd D3 even NC 31 32 TRACEDATA 19 D3 odd D2 even NC 33 34 TRACEDATA 17 D1 odd	D15 even	NC	7	8	TRACEDATA 31	D15 odd
D12 evenNC11111111111111D12 evenNC1314TRACEDATA 28D12 oddD11 evenNC1516TRACEDATA 27D11 oddD10 evenNC1718TRACEDATA 26D10 oddD9 evenNC1920TRACEDATA 25D9 oddD8 evenNC2122TRACEDATA 24D8 oddD7 evenNC2324TRACEDATA 23D7 oddD6 evenNC2526TRACEDATA 22D6 oddD5 evenNC2728TRACEDATA 21D5 oddD4 evenNC3132TRACEDATA 19D3 oddD2 evenNC3334TRACEDATA 18D2 oddD1 evenNC3536TRACEDATA 17D1 odd	D14 even	NC	9	10	TRACEDATA 30	D14 odd
D11 evenNC1516TRACEDATA 27D11 oddD10 evenNC1718TRACEDATA 26D10 oddD9 evenNC1920TRACEDATA 25D9 oddD8 evenNC2122TRACEDATA 24D8 oddD7 evenNC2324TRACEDATA 23D7 oddD6 evenNC2526TRACEDATA 22D6 oddD5 evenNC2728TRACEDATA 21D5 oddD4 evenNC2930TRACEDATA 20D4 oddD3 evenNC3132TRACEDATA 19D3 oddD2 evenNC3536TRACEDATA 17D1 odd	D13 even	NC	11	12	TRACEDATA 29	D13 odd
D10 evenNC1718TRACEDATA 26D10 oddD9 evenNC1920TRACEDATA 25D9 oddD8 evenNC2122TRACEDATA 24D8 oddD7 evenNC2324TRACEDATA 23D7 oddD6 evenNC2526TRACEDATA 22D6 oddD5 evenNC2728TRACEDATA 21D5 oddD4 evenNC2930TRACEDATA 20D4 oddD3 evenNC3132TRACEDATA 19D3 oddD2 evenNC3536TRACEDATA 17D1 odd	D12 even	NC	13	14	TRACEDATA 28	D12 odd
D9 evenNC1920TRACEDATA 25D9 oddD8 evenNC2122TRACEDATA 24D8 oddD7 evenNC2324TRACEDATA 23D7 oddD6 evenNC2526TRACEDATA 22D6 oddD5 evenNC2728TRACEDATA 21D5 oddD4 evenNC2930TRACEDATA 20D4 oddD3 evenNC3132TRACEDATA 19D3 oddD2 evenNC3334TRACEDATA 18D2 oddD1 evenNC3536TRACEDATA 17D1 odd	D11 even	NC	15	16	TRACEDATA 27	D11 odd
D8 evenNC2122TRACEDATA 24D8 oddD7 evenNC2324TRACEDATA 23D7 oddD6 evenNC2526TRACEDATA 22D6 oddD5 evenNC2728TRACEDATA 21D5 oddD4 evenNC2930TRACEDATA 20D4 oddD3 evenNC3132TRACEDATA 19D3 oddD2 evenNC3334TRACEDATA 18D2 oddD1 evenNC3536TRACEDATA 17D1 odd	D10 even	NC	17	18	TRACEDATA 26	D10 odd
D7 evenNC2324TRACEDATA 23D7 oddD6 evenNC2526TRACEDATA 22D6 oddD5 evenNC2728TRACEDATA 21D5 oddD4 evenNC2930TRACEDATA 20D4 oddD3 evenNC3132TRACEDATA 19D3 oddD2 evenNC3334TRACEDATA 18D2 oddD1 evenNC3536TRACEDATA 17D1 odd	D9 even	NC	19	20	TRACEDATA 25	D9 odd
D6 evenNC2526TRACEDATA 22D6 oddD5 evenNC2728TRACEDATA 21D5 oddD4 evenNC2930TRACEDATA 20D4 oddD3 evenNC3132TRACEDATA 19D3 oddD2 evenNC3334TRACEDATA 18D2 oddD1 evenNC3536TRACEDATA 17D1 odd	D8 even	NC	21	22	TRACEDATA 24	D8 odd
D5 evenNC2728TRACEDATA 21D5 oddD4 evenNC2930TRACEDATA 20D4 oddD3 evenNC3132TRACEDATA 19D3 oddD2 evenNC3334TRACEDATA 18D2 oddD1 evenNC3536TRACEDATA 17D1 odd	D7 even	NC	23	24	TRACEDATA 23	D7 odd
D4 evenNC2930TRACEDATA 20D4 oddD3 evenNC3132TRACEDATA 19D3 oddD2 evenNC3334TRACEDATA 18D2 oddD1 evenNC3536TRACEDATA 17D1 odd	D6 even	NC	25	26	TRACEDATA 22	D6 odd
D3 evenNC3132TRACEDATA 19D3 oddD2 evenNC3334TRACEDATA 18D2 oddD1 evenNC3536TRACEDATA 17D1 odd	D5 even	NC	27	28	TRACEDATA 21	D5 odd
D2 even NC 33 34 TRACEDATA 18 D2 odd D1 even NC 35 36 TRACEDATA 17 D1 odd	D4 even	NC	29	30	TRACEDATA 20	D4 odd
D1 even NC 35 36 TRACEDATA 17 D1 odd	D3 even	NC	31	32	TRACEDATA 19	D3 odd
	D2 even	NC	33	34	TRACEDATA 18	D2 odd
D0 even NC 37 38 TRACEDATA 16 D0 odd	D1 even	NC	35	36	TRACEDATA 17	D1 odd
	D0 even	NC	37	38	TRACEDATA 16	D0 odd

Bus and signal descriptions

- **TRACEDATA** Required. Data lines. This bus may be 8, 16, or 32 bits wide.
 - **TRACECTL** Required. 1 bit wide.
- **TRACECLK** Required. 1 bit wide.
- EXTOUT0 Optional. One of these signals is required when the decoder is in time-accurate mode. Time-accurate mode is a special mode that shifts decoded information from one state in the trace to an

earlier state in the trace. The purpose of this shifting is to show ARM11 instructions at the precise point in time when they were executed by the ARM11 processor, rather then the point in time when the associated ETM packet exited the ETM FIFO. Time-accurate mode is only useful if you want the logic analyzer to time correlate ARM11 instruction execution with trace data captured in a separate time domain on a separate logic analyzer card.

If you expect to use time-accurate mode, then EXTOUT0 or EXTOUT1 must be present, and must be driven high when the ETM detects a trigger. The recommended design is to use jumpers or zero-ohm resistors to allow the pins to be connected to GND or EXTOUT.

NC NC. Pins 1, 2, 3, and 4 must be true no-connects. Other NC signals can be left floating (no connects), or used to measure other signals of interest.

Other signals Optional. **The decoder ignores the signals shaded in blue.** These signals are routed to the connector to allow the connector to be used by RealView Trace. See the ARM *RealView ICE User's Guide* for detailed information on the requirements for these signals.

> These signals must be routed to a second, JTAG-only header so that they are accessible to a JTAG controller such as ARM's RealView ICE. See "Sharing the Connector Between Multiple Tools" on page 20 for a description of the second connector.

In addition, special consideration must be given to these signals so that the logic analyzer does not load them, such that they cannot be controlled by the JTAG controller. Use a 10 k Ω pullup resistor to avoid such loading. See the *Agilent Technologies E5346A 38-Pin Probe and E5351A 38-Pin Adapter Cable Installation Note* for information on how the probe loads the signals.

Connectors for ARM7/9

These connectors are designed to be used either with an Agilent logic analyzer *or* with ARM's RealView Trace. When used with the logic analyzer, the JTAG (run control) signals (shaded in blue) must be routed to a separate JTAG-only connector (page 20) so they are accessible to a JTAG controller such as ARM RealView ICE.

The signals shaded in blue are used by RealView Trace, but are not used by the logic analyzer.

Analyzer Pod	ETM Signal		r pin # view)	ETM Signal	Analyzer Pod
5V	NC	1	2	NC	12C
5V	NC	3	4	NC	12C
CLK even	GND	5	6	TRACECLK	CLK odd
D15 even	DBGRQ	7	8	MRDY or DBGACK	D15 odd
D14 even	nSRST	9	10	EXTTRIG	D14 odd
D13 even	TDO	11	12	VTRef	D13 odd
D12 even	RTCLK	13	14	Vsupply	D12 odd
D11 even	TCK	15	16	TRACEPKT 7	D11 odd
D10 even	TMS	17	18	TRACEPKT 6	D10 odd
D9 even	TDI	19	20	TRACEPKT 5	D9 odd
D8 even	nTRST	21	22	TRACEPKT 4	D8 odd
D7 even	TRACEPKT 15	23	24	TRACEPKT 3	D7 odd
D6 even	TRACEPKT 14	25	26	TRACEPKT 2	D6 odd
D5 even	TRACEPKT 13	27	28	TRACEPKT 1	D5 odd
D4 even	TRACEPKT 12	29	30	TRACEPKT 0	D4 odd
D3 even	TRACEPKT 11	31	32	TRACESYNC	D3 odd
D2 even	TRACEPKT 10	33	34	PIPESTAT 2	D2 odd
D1 even	TRACEPKT 9	35	36	PIPESTAT 1	D1 odd
D0 even	TRACEPKT 8	37	38	PIPESTAT 0	D0 odd

Normal trace port connector

Port size	MICTOR pins required
4	6, 38, 36, 34, 32, 30, 28, 26, 24
8	6, 38, 36, 34, 32, 30, 28, 26, 24, 22, 20, 18, 16
16	6, 38, 36, 34, 32, 30, 28, 26, 24, 22, 20, 18, 16, 37, 35, 33, 31, 29, 27, 25, 23

 Table 2
 Required signals (normal connector)

Bus and signal descriptions

TRACEPKT	Data lines. This bus may be 4, 8, or 16 bits wide.
TRACESYNC	Trace synchronization signal. 1 bit wide.
PIPESTAT	Pipeline status. 3 bits wide.
NC	Pins 1, 2, 3, and 4 must be true no-connects. Other NC signals can be left floating (no connects), or used to measure other signals of interest.
Other signals	Optional. The decoder ignores the signals shaded in blue. These signals are routed to the connector to allow the connector to be used by RealView Trace. See the ARM <i>RealView ICE User's</i> <i>Guide</i> for detailed information on the requirements for these signals.
	These signals must be routed to a second, JTAG-only header so that they are accessible to a JTAG controller such as ARM's RealView ICE. See "Sharing the Connector Between Multiple Tools" on page 20 for a description of the second connector.
	In addition, special consideration must be given to these signals so that the logic analyzer does not load them, such that they cannot be controlled by the JTAG controller. Use a 10 k Ω pullup resistor to avoid such loading. See the <i>Agilent Technologies</i> <i>E5346A 38-Pin Probe and E5351A 38-Pin Adapter Cable</i> <i>Installation Note</i> for information on how the probe loads the signals.

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Analyzer Pod	ETM Signal		r pin # /iew)	ETM Signal	Analyzer Pod
5V	NC	1	2	NC	12C
5V	NC	3	4	NC	12C
CLK even	GND	5	6	TRACECLK	CLK odd
D15 even	DBGRQ	7	8	MRDY or DBGACK	D15 odd
D14 even	nSRST	9	10	EXTTRIG	D14 odd
D13 even	TDO	11	12	VTRef	D13 odd
D12 even	RTCLK	13	14	Vsupply	D12 odd
D11 even	TCK	15	16	NC	D11 odd
D10 even	TMS	17	18	NC	D10 odd
D9 even	TDI	19	20	TRACEPKT 14, TRACEPKT 15	D9 odd
D8 even	nTRST	21	22	TRACEPKT 12, TRACEPKT 13	D8 odd
D7 even	NC	23	24	TRACEPKT 10, TRACEPKT 11	D7 odd
D6 even	NC	25	26	TRACEPKT 8, TRACEPKT 9	D6 odd
D5 even	NC	27	28	TRACEPKT 6, TRACEPKT 7	D5 odd
D4 even	NC	29	30	TRACEPKT 4, TRACEPKT 5	D4 odd
D3 even	NC	31	32	TRACEPKT 0, TRACEPKT 3	D3 odd
D2 even	NC	33	34	PIPESTAT 2, TRACEPKT 2	D2 odd
D1 even	NC	35	36	PIPESTAT 1, TRACEPKT 1	D1 odd
D0 even	NC	37	38	PIPESTAT 0, TRACESYNC	D0 odd

Multiplexed trace port connector

 Table 3
 Required signals (multiplexed connector)

Port size	MICTOR pins required
4	6, 38, 36, 34, 32
8	6, 38, 36, 34, 32, 30, 28
16	6, 38, 36, 34, 32, 30, 28, 26, 24, 22, 20

See for page 15 for descriptions of the signals.

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Analyzer Pod	ETM Signal		r pin # view)	ETM Signal	Analyzer Pod
5V	NC	1	2	NC	12C
5V	NC	3	4	NC	12C
CLK even	GND	5	6	TRACECLK	CLK odd
D15 even	DBGRQ	7	8	MRDY or DBGACK	D15 odd
D14 even	nSRST	9	10	EXTTRIG	D14 odd
D13 even	TDO	11	12	VTRef	D13 odd
D12 even	RTCLK	13	14	Vsupply	D12 odd
D11 even	TCK	15	16	NC	D11 odd
D10 even	TMS	17	18	NC	D10 odd
D9 even	TDI	19	20	NC	D9 odd
D8 even	nTRST	21	22	NC	D8 odd
D7 even	TRACEPKT_B3	23	24	TRACEPKT_A3	D7 odd
D6 even	TRACEPKT_B2	25	26	TRACEPKT_A2	D6 odd
D5 even	TRACEPKT_B1	27	28	TRACEPKT_A1	D5 odd
D4 even	TRACEPKT_B0	29	30	TRACEPKT_A0	D4 odd
D3 even	TRACESYNC_B	31	32	TRACESYNC_A	D3 odd
D2 even	PIPESTAT_B2	33	34	PIPESTAT_A2	D2 odd
D1 even	PIPESTAT_B1	35	36	PIPESTAT_A1	D1 odd
D0 even	PIPESTAT_B0	37	38	PIPESTAT_A0	D0 odd

Demultiplexed trace port connector (Port size = 4)

Port size	Use these connectors
4	Use the connector shown here.
8	Use two "Normal" 8 -bit connectors but only one TRACECLK.
16	Use two "Normal" 16-bit connectors but only one TRACECLK.

 Table 4
 Demultiplexed connectors

Bus and signal descriptions

TRACEPKT_A	Data lines for Port A. This bus may be 4, 8, or 16 bits wide.
TRACESYNC_A	Trace synchronization signal for Port A. 1 bit wide.
PIPESTAT_A	Pipeline status for Port A. 3 bits wide. See PIPESTAT Symbols for more information.
TRACEPKT_B	Data lines for Port B. This bus may be 4, 8, or 16 bits wide.
TRACESYNC_B	Trace synchronization signal for Port B. 1 bit wide.
PIPESTAT_B	Pipeline status for Port B. 3 bits wide. See PIPESTAT Symbols for more information.
NC	Pins 1, 2, 3, and 4 must be true no-connects. Other NC signals can be left floating (no connects), or used to measure other signals of interest.
Other signals	Optional. The decoder ignores the signals shaded in blue. These signals are routed to the connector to allow the connector to be used by RealView Trace. See the ARM <i>RealView ICE User's</i> <i>Guide</i> for detailed information on the requirements for these signals.
	These signals must be routed to a second, JTAG-only header so that they are accessible to a JTAG controller such as ARM's RealView ICE. See "Sharing the Connector Between Multiple Tools" on page 20 for a description of the second connector.
	In addition, special consideration must be given to these signals so that the logic analyzer does not load them, such that they cannot be controlled by the JTAG controller. Use a 10 k Ω pullup resistor to avoid such loading. See the <i>Agilent Technologies</i>

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E5346A 38-Pin Probe and E5351A 38-Pin Adapter Cable Installation Note for information on how the probe loads the signals.

Sharing the Connector Between Multiple Tools

The standard header defined in this document is designed to be used with RealView Trace (JTAG run-control and trace) or a logic analyzer (trace only).

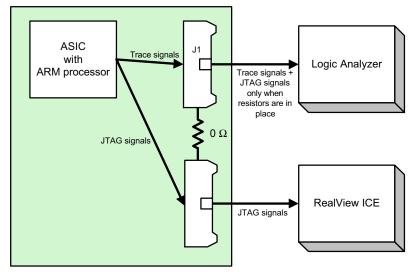
The logic analyzer ignores the JTAG signals. These signals must be routed to a second, JTAG-only header so that they are accessible to a JTAG controller such as ARM's RealView ICE. In addition, special consideration must be given to these signals so that the logic analyzer does not load them, such that they cannot be controlled by the JTAG controller.

See the ARM *RealView ICE User's Guide* for further information on the requirements for the JTAG signals. See the *Agilent Technologies E5346A 38-Pin Probe and E5351A 38-Pin Adapter Cable Installation Note* for information on how the probe loads the signals.

There are three possible ways to provide these signals to RealView ICE and at the same time, prevent the logic analyzer from interfering with their use.

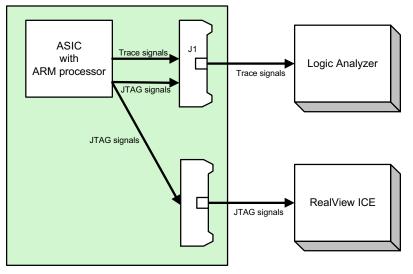
Option 1: Chained connectors

Route the JTAG signals to two connectors on the board: first to a JTAG-only 2X10 berg connector, then to J1. Place zero-ohm resistors between the two connectors. Leave the zero-ohm resistors in place when using J1 with RealView Trace. Remove the resistors when using J1 with the logic analyzer.



Option 2: Independent connectors

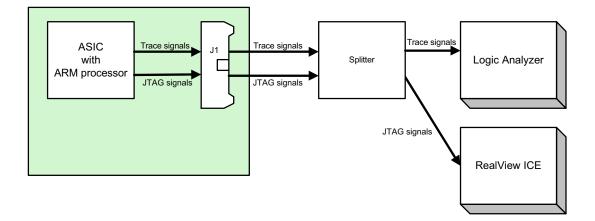
Route the JTAG signals to two connectors. Provide 10 $k\Omega$ pull-up resistors on the signals (particularly nSRST) so that the logic analyzer does not pull these signals to ground.



Option 3: Splitter board

Route the JTAG signals to one connector (J1) and use a splitter board such as Agilent product number E9595A Option 002 to provide the JTAG-only connector for RealView ICE.





2 Designing Your Board

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